PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

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PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(PCT Rule 71.1)

Date of mailing *(day/month/year)*	22.10.2004
Applicant's or agent's file reference 03F015-PCT	**IMPORTANT NOTIFICATION**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/JP 03/07673	17.06.2003	20.06.2002

Applicant
TOKYO ELECTRON DEVICE LIMITED et al.

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary report on patentability and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary report on patentability. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

The applicant's attention is drawn to Article 33(5), which provides that the criteria of novelty, inventive step and industrial applicability described in Article 33(2) to (4) merely serve the purposes of international preliminary examination and that "any Contracting State may apply additional or different criteria for the purposes of deciding whether, in that State, the claimed inventions is patentable or not" (see also Article 27(5)). Such additional criteria may relate, for example, to exemptions from patentability, requirements for enabling disclosure, clarity and support for the claims.

Name and mailing address of the international preliminary examining authority:	Authorized Officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	MONTANES VILLANUEVA Tel. +49 89 2399-2934

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 03F015-PCT	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/JP 03/07673	International filing date *(day/month/year)* 17.06.2003	Priority date *(day/month/year)* 20.06.2002
International Patent Classification (IPC) or both national classification and IPC G06F12/02		
Applicant TOKYO ELECTRON DEVICE LIMITED et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 5 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the opinion
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
29.07.2004	22.10.2004
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer Weber, R Telephone No. +49 89 2399-2655

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/JP 03/07673

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:

Description, Pages

1-28	as originally filed

Claims, Numbers

3 (part), 4-7, 8 (part), 12 (part)	as originally filed
1, 2, 3 (part), 8 (part), 9-11, 12 (part)	received on 29.07.2004 with letter of 29.07.2004

Drawings, Sheets

1-5, 7-11	as originally filed
6	received on 29.07.2004 with letter of 29.07.2004

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).

   ☐ the language of publication of the international application (under Rule 48.3(b)).

   ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   ☐ contained in the international application in written form.

   ☐ filed together with the international application in computer readable form.

   ☐ furnished subsequently to this Authority in written form.

   ☐ furnished subsequently to this Authority in computer readable form.

   ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   ☐ the description, pages:

   ☐ the claims, Nos.:

   ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	
	No:	Claims	1-12
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-12
Industrial applicability (IA)	Yes:	Claims	1-12
	No:	Claims	

2. Citations and explanations

   see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Reference is made to the following document:
D1 : WO00/49488

The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 1-12 is not new in the sense of Article 33(2) PCT.

The document D1 discloses the features of all claims as indicated in the following table:

PCT JP03/07672		D1 : WO00/49488	
claims claim(lines)	**clarity**	**passages** page(lines)	**comments**
1(4-7)	the redundancy portion contains ECC, a logical address and a valid flag according to page 8(16)-10(14) and fig.2 of the description	fig.2 fig.1; 20(14-25); fig.11; 42(7)-43(5); 60(14-23); fig.3.4 28(1-19);	a controller 8 controls a non-volatile flash memory 5, which is divided into blocks; each block 4 may comprise physical pages each to store one logical page (= sector) e.g. 1,2,3...; or each block may comprise physical pages each to store a plurality of logical pages (= sectors) e.g. 0,1,2,3 each page (= sector) has a redundancy portion to store ECC, the logical host address LA and a flag "Data Structure Type" to indicate, among others, valid "Data Sector" or "Deleted Data Sector "
1(8-14)		fig.23; 50(16)-51(15)	the controller, when writing to the flash memory and when an existing valid data is found in a physical sector VA corresponding to the logical sector address LA (steps 150,152,156,157,161), marks said data as "Obsolete" (step 159) before writing the data into a new empty physical sector (step 166)
2		fig.22; 49(31)-50(14)	a sector may be readout

3 [page 29/1(20-25)]		50(24-27); 46(12-23); 2(23-29) 3(4-18); 9(31)-10(27); 26(28)-27(12)	a table SAT is used to translate a logical sector address LA to a physical sector address VA; the SAT table is stored in the flash memory but some more recent translations are only stored in tables WSL, WBL in a (S)RAM memory
3 [page 29/1(25)-page 29/2(1)]		2(9-16) fig.23; 50(34)-51(4); 31(28)-32(12)	a write pointer WP points to the physical address of an empty sector where new data should be written at a corresponding logical sector address (steps 158-166); the write pointer is stored in a volatile memory since it must be stored into a TLB for backup each time the SAT table is updated with the last recent translations from the tables WSL, WBL
3 [page 29/2(2-4)		10(32)-11(8); 27(14-25) 53(28)-54(32)	at initiation of the flash memory the write pointer WP and the last not yet saved translations in WSL and WBL tables are restored into the (S)RAM by scanning the logical addresses from the redundancy portions 20 of the last written sectors in the flash memory (thus avoiding generalised scanning of all sectors)
3 [page 29/2(5)-30(4)]		2(17-29); 50(34)-51(4)	the controller writes new data into said empty sector pointed to by said write pointer WP and updates the address translation tables WSL, WBL
4		51(2-4,14-15)	the valid flags of the old and the new sector are adapted respectively to valid and obsolete (empty)
5		20(20-25); 7(17-21) 22(26-30)	all sectors stored in a block are erased simultaneously; before a block is erased, the sectors which are still valid are transferred into empty sectors in another block
6			see for same features in claim 2
7		fig.3,4 28(1-19)	a header portion 1b is added to each data sector 1a in the flash memory; the header has among others a field 20 which indicates that the sector contains valid "Data Sector" or obsolete "Deleted Data Sector"
8			see for same features in claim 2
9			see for same features in claim 1
10			see for same features in claim 4
11			see for same features in claim 5

12		fig.2	the controller 8 being a general microprocessor, all flowcharts of the cited figures 17,22,23 are clearly implemented by program; for the remaining features see for the same features in claim 1

CLAIMS

1. (Amended) A memory device characterized by comprising:

a non-volatile memory (11) including a plurality of memory blocks which stores data and each of which is comprised of one or more physical pages each including one or more logical pages and a redundancy portion; and

a controller (12, S314, S308 to S310) which, when to-be-written data is supplied to said memory device, writes said to-be-written data in that empty logical page in said logical pages which is in a data storable state, discriminates whether to-be-replaced data to be replaced with said to-be-written data is stored in said logical pages, and writes validity data indicating that said to-be-replaced data is not valid in that physical page which includes said logical page that stores said to-be-replaced data, when having discriminated that said to-be-replaced data is stored in said logical page.

2. The memory device according to claim 1, characterized in that when information for specifying a to-be-read logical page to be read out is supplied to said memory device, said controller (12) specifies said to-be-read logical page based on said information, reads data from said specified to-be-read logical page and sends said read data outside (S201 to S214).

3. (Amended) The memory device according to claim 1, characterized in that physical addresses are allocated to said logical pages,

said memory device further comprises a second memory (123) which is randomly accessable and stores an address translation table representing a correlation between said physical addresses of said logical pages and logical addresses to be used to specify said logical pages by an external unit, and a third memory (123) which is randomly accessable and stores a write pointer that points the empty logical page in said logical pages which is in a data storable state and instructs the physical address of said specified empty logical

page,

when this memory device is activated, said controller reads the redundancy portions of said non-volatile memory and prepare the address translation table in said second memory and the write pointer in said third memory;

and

when to-be-written data and a logical address are supplied to said memory device,

information, reads data from said specified to-be-read logical page and sends said read data outside (S201 to S214).

9. (Amended) A memory managing method of managing a non-volatile memory (11) including a plurality of memory blocks which stores data and each of which is comprised of one or more physical pages each including one or more logical pages and a redundancy portion, characterized by comprising the steps of:

writing, when to-be-written data is supplied to said memory, said to-be-written data in that empty logical page in said logical pages which is in a data storable state (S314); and

discriminating whether to-be-replaced data to be replaced with said to-be-written data is stored in said logical pages, and writing validity data indicating that said to-be-replaced data is not valid in that physical page which includes said logical page that stores said to-be-replaced data, when it is discriminated that said to-be-replaced data is stored in said logical page (S308 to S310).

10. The memory managing method according to claim 9, characterized in that validity data indicating that said written to-be-written data is valid is written in that physical page which includes the logical page where said to-be-written data is stored (S314), that logical page where data is not stored is specified based on said validity data and said specified logical page is treated as said empty logical page.

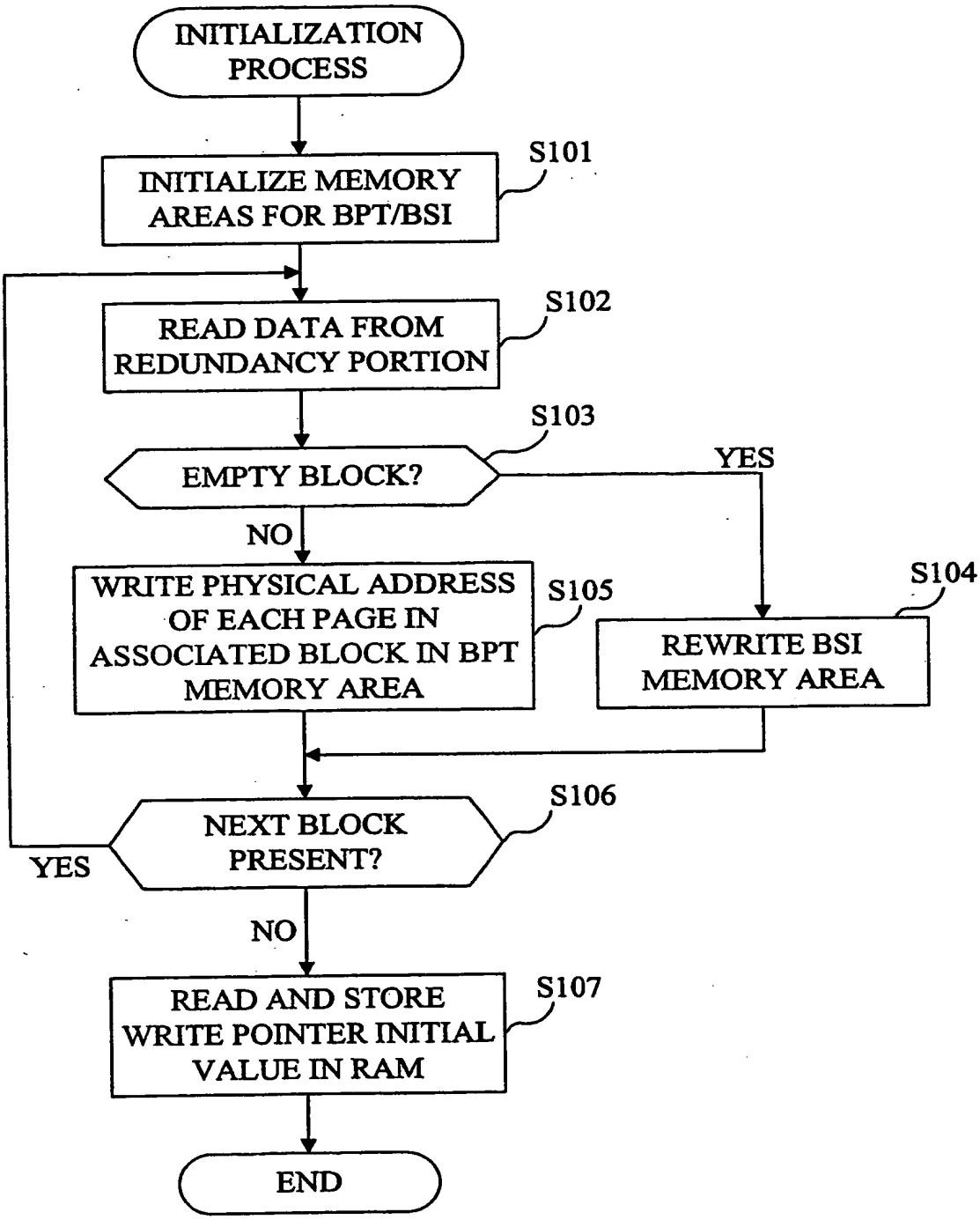
11. (Amended)The memory managing method according to claim 10, characterized by further comprising the steps of: discriminating whether or not data stored in each of said logical pages in to-be-erased memory blocks is valid based on said validity data (S501), specifying a logical pages which are located in another memory blocks and where data is not stored, transferring the data which has been discriminated as valid into said specified logical pages (S502 and S503, S507), and erasing data stored in said to-be-erased memory blocks (S504).

12. (Amended)A program for allowing a computer (121), connected to a non-volatile memory (11) including a plurality of memory blocks which stores data and each of

which is comprised of one or more physical pages each including one or more logical pages and a redundancy portion, to function to:

6/11

FIG. 6


INITIALIZATION PROCESS
INITIALIZE MEMORY AREAS FOR BPT/BSI
S101
READ DATA FROM REDUNDANCY PORTION
S102
EMPTY BLOCK?
S103
YES
NO
WRITE PHYSICAL ADDRESS OF EACH PAGE IN ASSOCIATED BLOCK IN BPT MEMORY AREA
S105
REWRITE BSI MEMORY AREA
S104
NEXT BLOCK PRESENT?
S106
YES
NO
READ AND STORE WRITE POINTER INITIAL VALUE IN RAM
S107
END